Bias Resistor Transistors

NPN Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

FEATURES

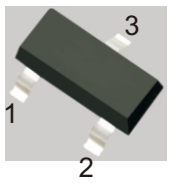
- Reduces board space
- Simplifies Circuit Design
- Reduces Board Space and Component Count
- Qualified to AEC-Q101 Standards for High Reliability

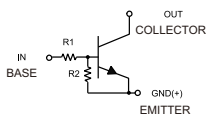
Mechanical Data

- Case: SOT-23
- R_1 = 10KΩ (Typ) , R_2 = 10KΩ (Typ)

PINNING

PIN	DESCRIPTION
1	BASE
2	EMITTER
3	COLLECTOR





Simplified outline SOT-23 and symbol

Automotive Grade

MAXIMUM RATINGS (Ta =25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	50	V
Collector-Emitter Voltage	V_{CEO}	50	V
Output current	I_C	500	mA
Power dissipation	P_D	200	mW
Thermal Resistance – Junction-to-Ambient	R_{thJA}	625	°C/W
Junction temperature	T_J	-55~ +150	°C
Range of storage temperature	T_{stg}	-55~ +150	°C

ELECTRICAL CHARACTERISTICS (TA = 25°C unless otherwise noted.)

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Collector-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10uA , I_E = 0	50			V
Collector-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 2mA , I_B = 0	50			V
Emitter-base breakdown voltage	$V_{(BR)EBO}$	I_E = 1mA , I_C = 0	10			V
Collector-Base Cut off Current	I_{CBO}	V_{CB} = 50V , I_E = 0			100	nA
Collector-Emitter Cut off Current	I_{CEO}	V_{CE} = 50V , I_B =0			0.5	uA
Emitter-Base Cutoff Current	I_{EBO}	V_{EB} = 5V , I_C =0			0.5	mA
DC Current Gain	h_{FE}	V_{CE} = 5V , I_C =50mA	56			
Output Voltage (on)	V_{OL}	V_{CE} = 5.0V , V_{BE} = 2.5V , R_L = 1.0KΩ			0.2	V
Output Voltage (on)	V_{OH}	V_{CE} = 5.0V , V_{BE} = 0.5V , R_L = 1.0KΩ	4.9			V
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	I_C = 50mA , I_B = 2.5mA			0.3	V
Input Voltage(off)	$V_{I(off)}$	V_{CE} = 5V , I_C =100μA	0.5			V
Input Voltage(on)	$V_{I(on)}$	V_{CE} = 0.3V , I_C =10mA			3	V
Input resistance	R_1		7	10	13	KΩ
Input resistance	R_2		7	10	13	KΩ
Resistance ratio	R_2/ R_1		0.8	1	1.2	

Typical Performance Characteristics

Fig 1. HFE vs. IC

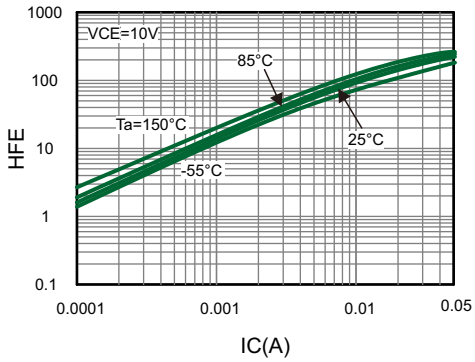


Fig 2. Vin vs. IC

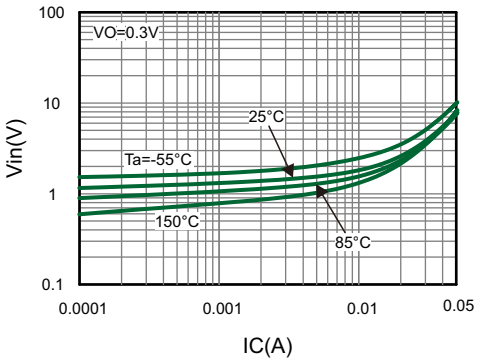


Fig 3. IC vs. Vin

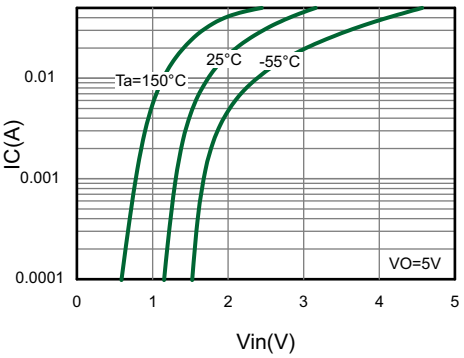


Fig 4. VCE(sat) vs. IC

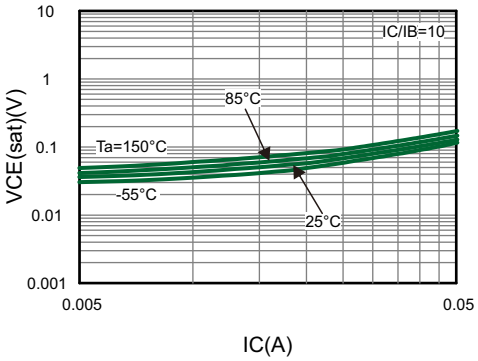
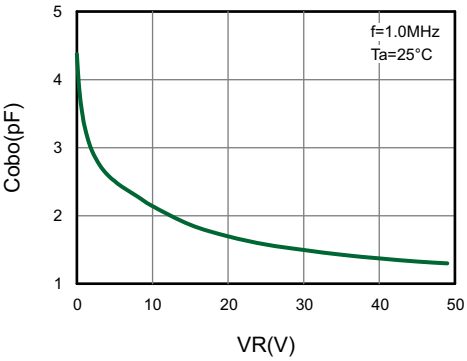
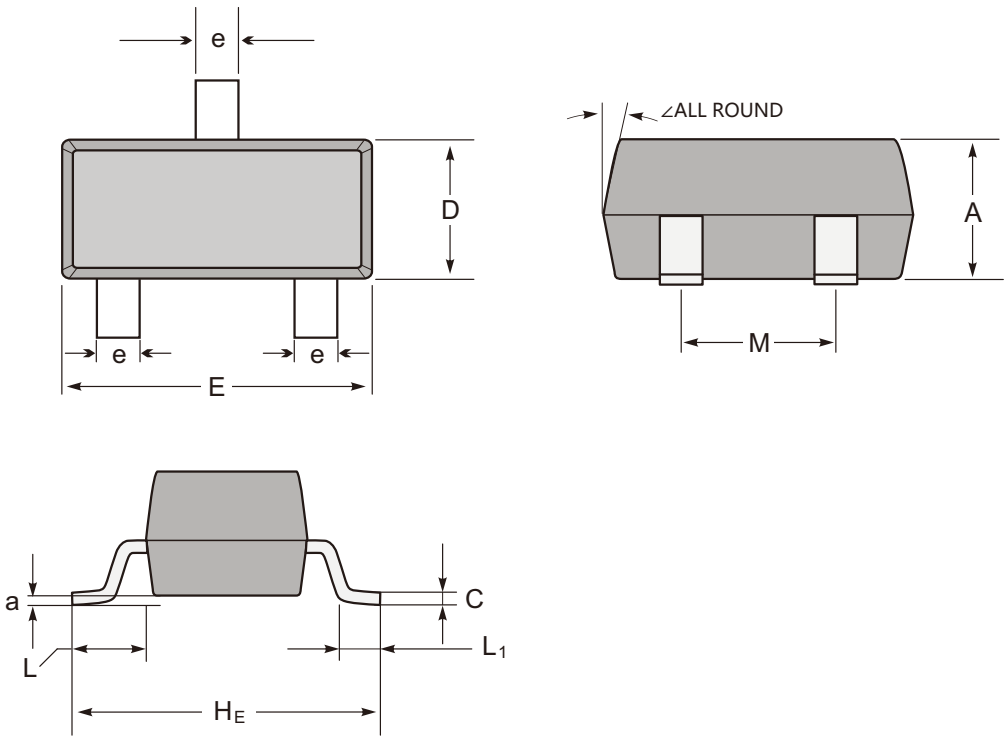


Fig 5. Capacitance



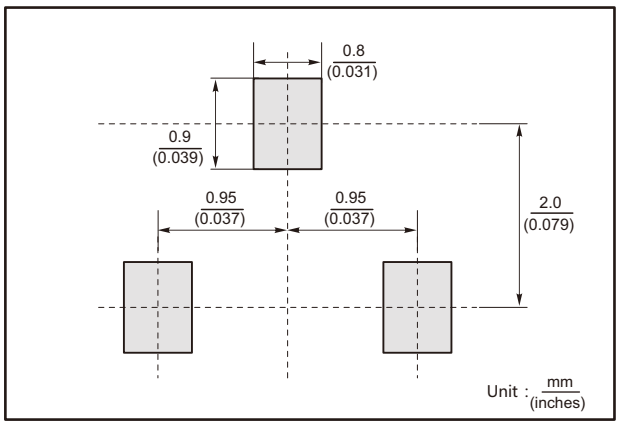
SOT-23 Package Outline Dimensions



SOT-23 mechanical data

UNIT		A	C	D	E	H_E	e	M	L	L_1	a	∠
mm	max	1.1	0.20	1.4	3.0	2.6	0.6	1.95	0.55 (ref)	0.36 (ref)	0.15	12°
	min	0.9	0.08	1.2	2.8	2.2	0.35	1.7			0.0	
mil	max	43	7.9	55	118	102	24	77	22 (ref)	14 (ref)	6	
	min	35	3.1	47	110	87	13	67			0.0	

The recommended mounting pad size



Marking

Type number	Marking code
JDTD114EWD	14E

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